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CS 141: Computing Hardware

Lab 3 part1 : Traffic Light Controller

Testing methodology

The MIPS datapath is implemented to support just R types (except for jr which will be implemented later along with J types). The following blocks are implemented as modules and instantiated in the MIPS core module:

1. Control
2. ALU control
3. ALU
4. PC Register
5. Register File
6. IorD mux
7. IR register
8. MDR register
9. RegDst mux
10. MemtoReg mux
11. A register
12. B register
13. ALUSrcA 3 to 1 mux
14. ALUSrcB 5 to 1 mux
15. PCSource 3 to 1 mux
16. ALUout register

The Control FSM module is tested by creating a testbench that resets the FSM and runs it for about 100 clock cycles. The waveform of the enable pins(*IRWrite, MemWrite RegWrite, PCWriteCond*) and select pins(*IorD, ALUSrcA, ALUSrcB, ALUOp, PCSource, RegDst,*

*MemtoReg*) are then observed in each state and checked for consistency with the MIPs R type FSM diagram.

In order to test for functionality of the entire datapath we convert the following assembly code to machine code and load it into the instruction memory:

We then view the waveform of the 32 registers in the Register File and check whether they hold store the following values: